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Product Alert

Product Name: **FireBridge 82C814 PCI Bridge**

Title: **Deadlock Prevention**

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Scope

This document provides information on enabling and using the deadlock prevention mechanism of the 82C814 PCI-CardBus Bridge, revisions 1.0 and 1.2. These OPTi chips are identified by a four-digit code of “10UE” or “12UE” (respectively) that is stamped on the top side of the chip.

Issue

The 82C814 silicon implements a deadlock prevention mechanism that works as follows.

Downstream cycles (from the primary PCI bus to the secondary bus) are always given priority in the 82C814 design. When a secondary bus master attempts to do a read or write cycle to a primary target at the same time as a primary bus master is attemping a downstream access, the secondary bus master is retried until the primary-to-secondary bus access completes.

There are certain situations that arise where a secondary bus master will not allow access to its registers until it has completed a previously initiated upstream bus master transfer. Both primary and secondary PCI buses generate retry cycles indefinitely in this case, and deadlock will result if no other action is taken.

This failure scenario appears primarily in systems with other PCI-PCI bridges such as the Intel 810 chipset, whose external PCI bus is actually the secondary bus of an internal PCI-PCI bridge.

Solution

The 82C814 architecture incorporates a retry counter that keeps track of the number of times a primary bus master is retried. Depending on how the registers are programmed, it can either:

- Automatically resolve the deadlock by temporarily reversing the priority
- Signal the deadlock condition on SERR# to allow system firmware to handle the condition.

All current applications expect the deadlock to be resolved automatically, so the necessary register programming for automatic mode is described below. Along with this are mentioned two additional bits that should be set at the same time for best operation.

1. Set PCICFG 5Eh[7] = 1: Enables the deadlock prevention feature.
2. Set PCICFG 5Fh[1] = 1: Sets the number of retries before reversing priority to 8. Note that this register is **write-only**, so it will always read back 00h regardless of the values programmed. For this application, all of the other register bits can be written to 0.
3. Set PCICFG 5Eh[5] = 1: Enables the upstream posted write buffer for efficient operation.
4. Set PCICFG 5Eh[4] = 1: Selects the proper voltage scaling for input buffers. This setting is acceptable for use on designs supplying either 3.3V or 5V to the core.

These settings are sufficient for normal operation in generic PCI add-in card applications.

Software Implementation

These changes can be effected under Microsoft Windows, using different methods according to the version of the operating system in use. Refer to OPTi Product Alert PA062 for details.